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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/903,453	07/29/97	FORBES	L 303.378US1

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EXAMINER	
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ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No. 08/903,453	Applicant(s) Forbes et al.
	Examiner George C. Eckert II	Group Art Unit 2815

☒ Responsive to communication(s) filed on *Feb 16, 2000*.

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-6 and 20-64* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-6 and 20-64* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *16 & 18*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Response to Amendment

Applicants' amendment dated February 16, 2000 in which claim 38 was amended, and claims 39-64 were added has been entered of record as Paper No. 17.

Election

Applicant's election **without** traverse of Group I, claims 1-6 in Paper No. 10 is acknowledged.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-6 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11-18 of co-pending Application No. 08/902,843. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present invention and co-pending Application no. 08/902,843 disclose a transistor having:

a source and a drain separated by a channel supported by a semiconductor substrate;

a floating gate formed between the source and the drain above the channel and separated by an insulative amorphous carburized silicon layer;

a control gate formed adjacent to and insulated from the floating gate;

wherein the transistor is part of a memory cell comprising a capacitor.

Further, stacked capacitors are well known and widely used in memory devices.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 4, 5, 20, 23, 29, 32 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakata et al., *Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device structures*, Electronics Letters, April 28, 1994, Vol. 30, No. 9.

With regard to claim 4, Sakata et al. teach in figure 1, a capacitive device comprising:

a first conductor layer shown as the a-Si:H layer which is supported by the substrate;

a dielectric layer of amorphous silicon carbide, shown as the a-SiC:H layer, formed on top of the first conductor layer; and

a second conductor layer shown as metal and formed on top of the dielectric layer.

With regard to claim 5, Sakata et al. teach that the layers extend substantially vertically from a general surface of the substrate. With regard to claim 20, Sakata et al. teach that the device may be used in a floating gate memory device (last paragraph in first column on page 688) wherein the a-Si:H layer is a floating gate and a layer of amorphous silicon carbide is between the floating gate and the substrate. With regard to claim 23, Sakata et al. teach under *Sample preparation* that the substrate is crystalline silicon doped n- or p-type. With regard to claims 29, 32 and 36, Sakata et al. teach the first conductive layer of a-Si:H supported by the substrate, the layer of amorphous SiC:H there over, and a second conductive layer of metal over the layer of a-SiC:H. The different intended uses cited in the preambles of these claims are not sufficient to establish patentability over that taught by Sakata et al., since the device of Sakata et al. is a semiconductor device which may be used as a memory cell and is inherently capacitive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6, 21, 22, 24-30, 33-34, 37, 39, 41, 44-46 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata et al. With regard to these claims and as discussed above, Sakata et al. have taught the structure of a floating gate device having a doped monocrystalline silicon substrate, a graded amorphous silicon carbide layer thereon, an amorphous silicon layer to serve as a floating gate, a second amorphous silicon carbide layer thereon, and a metal layer to serve as a control gate. Sakata et al. do not expressly disclose the device comprising source, drain or channel regions. However, because Sakata et al. do teach that the device can be applied as a memory device, specifically a floating gate device, these features are considered obvious. Sakata et al. further state on page 689 that the device can be used as a dynamic random access memory (DRAM). Both a floating gate device (typically used as an erasable programmable read only memory device or EPROM) and a DRAM device comprise source/drain and channel regions to effect a transistor capable of memory functions. Also, it is well known in the art that appropriate circuitry such as word lines and bit lines are required to effect a memory array.

Regarding the limitations that the substrate comprises a semiconductor surface layer on an underlying insulating portion, such limitation is also considered obvious. Placing a semiconducting layer on an underlying insulating layer results in a device commonly referred to as silicon-on-insulator (SOI). By placing the semiconducting layer above an insulator, several advantages are realized. SOI reduces capacitive coupling between various circuit elements over the entire IC

chip, reduces chip size and/or increases packing density, and minimum device separation is determined only by the limitations of lithography. Therefore the claimed limitations that the device be formed over an underlying insulating portion are also considered obvious changes over that taught by Sakata et al.

Finally, the limitations that the substrate is p-type while the source and drain regions are n-type, are considered obvious over that taught by Sakata et al. First, Sakata et al. teach that the substrate may be formed having a p-type conductivity (see column 2, under *Sample preparation*). As such, because it is well known that a transistor formed in a p-type substrate will also be formed with n-type source/drain regions (to form an NMOS transistor), those limitations in the instant claims are considered obvious.

Claims 31, 35, 38, 40, 42, 43, 47-49 and 51-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata et al. as applied above, and further in view of Sugita et al. (of record). Sakata et al. taught the device of claims 1, 2, 3, 21, 29, 32, 36, 46 and 50 as discussed above. However, the device was not taught wherein the conductive layers which constitute the floating and control gates comprise polysilicon. Sugita et al. teaches a device using a silicon carbide insulator wherein the floating gate 6 is polysilicon. Polysilicon is well known as a gate conductor in the art. Its use as the control gate electrode is considered an obvious change over that taught by Sakata et al., especially in light of the use of polysilicon as a floating gate as taught by Sugita et al.

Sakata et al. and Sugita et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the polysilicon as taught by Sugita et al. in the device of Sakata et al. The motivation for doing so is that polysilicon is a well known conductor in the art as established by Sugita et al. Therefore, it would have been obvious to combine Sakata et al. with Sugita et al. to obtain the invention of claims 31, 35, 38, 40, 42, 43, 47-49 and 51-64.

Response to Arguments

Applicant's arguments filed February 16, 2000 have been fully considered but they are not persuasive. Regarding the rejection of claims under 35 USC §102, Applicants arguments are directed to claim 20 which claims, in full, "A memory cell comprising: a floating gate; and a layer of amorphous carburized silicon between the floating gate and a substrate."

Applicants state and primarily direct their argument to the purported fact that "Sakata does not disclose a gate." This contention is not seen. Sakata et al. state in their first column on page 688 that they "propose and experimentally confirm that the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." (Emphasis added). Sakata et al. then teach the formation and testing of the device of Fig. 1 under *Sample preparation* and *Results and discussion*. Under these sections, Sakata et al. refer to the device as a diode. However, nowhere do Sakata et al. teach that the structure of Fig. 1 or the test figure must somehow be altered to be considered a "floating gate" device. Rather, Sakata et al. teach that, in the "diode" test structure

of Fig. 1, "the presence of the undoped a-Si:H layer sandwiched between the a-SiC:H layers is essential for obtaining a large memory window." This is the confirmation that Sakata et al. discussed in the first column, that the layer of a-Si:H in the "diode" structure behaves as a "floating gate" in that charge is stored thereon.

Applicants further state that "[a] gate is known to those skilled in the art as a continuous, electrically conductive structure" in what appears to be a contrast to that stated by Applicants regarding the structure of Sakata et al. that "a-Si:H [is a] highly resistive, insulating layer[.]" However, such limitation regarding the resistivity of the floating gate is not included in claim 20. Secondly, use of the term "floating gate" does not import an inherent, specific resistivity which is common to all floating gates in the art. Rather, what is inherent to all floating gates is that they are layers formed in a memory cell and used to store charge. This is what the continuous, a-Si:H layer of Sakata et al. does.

Applicants also point out that there is only speculation in the Sakata et al. article as to how the device of Fig. 1 works. Specifically that Sakata et al. "speculate that traps in the a-Si:H and/or at the interface between a-Si:H and a-SiC:H are acting as memory sites" and that "[t]he storage mechanism in the diode structure disclosed by Sakata is a product of pure speculation, and therefore, Sakata does not disclose a gate." However, it is well established that even though Applicants may have discovered a better explanation for why or how the structure works, such knowledge does not negative the fact that the structure previously existed. Atlas Powder Co. v IRECO Inc., 51 USPQ2d 1943, 1946-47 (Fed. Cir. 1999) (citing Titanium Metal Corp. v.

Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (the discovery of a previously unappreciated property of a prior art composition, or of a scientific explanation for the prior art's functioning, does not render the old composition patentably new to the discover.).

In sum, it is simply not seen that the device of Sakata et al, as shown in Fig. 1 and discussed throughout the article, does not form a "floating gate." What is taught is that Sakata et al. have formed a memory cell comprising a floating gate over a substrate with a layer of amorphous silicon carbide therebetween. This anticipates the limitations of claim 20 and the rejection is maintained.

Regarding the rejections of claims under 35 USC §103(a), Applicants state that there is no teaching or motivation to include the limitations not taught by the primary reference, here being Sakata et al. Applicants first contend that the limitation of a floating gate is not taught by Sakata et al. and that such limitation would not be obvious. However, the floating gate limitation was discussed in detail above and applies here as well.

Applicants second contention is that Sakata et al. do not make obvious the use of source, drain and channel regions. However, such regions are the basis of what makes a transistor function and considered obvious to those of ordinary skill in the art. Furthermore, Sakata et al. teach on page 689 under *Conclusion* that the proposed heterojunction structure can be applied to electrically programmable and erasable memory devices (e.g EEPROMs). Without source, drain and channel regions, these devices would have limited application and not enjoy their widespread

use in the industry. The inclusion of source, drain and channel regions is therefore considered obvious and the rejections are maintained.

Finally, Applicants argue that the combination of Sakata et al. with Sugita is unfounded and repeat arguments regarding Sakata's purported failure to disclose a floating gate and mere speculation as to the operation of their device. These arguments have been addressed above and are hereby incorporated. Lastly, Applicants state that there is no suggestion to combine Sakata and Sugita however, the reason for combination was included in the previous rejection and made again above. The arguments are not persuasive and the rejections are maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ms. Mahshid Saadat, can be reached on (703) 308-4915. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GCE
May 5, 2000

DAVID HARDY
PRIMARY EXAMINER